MASTER COURSE OUTLINE
Prepared By: Julie Chang Date: Sep 2017

COURSE TITLE
Design of Logic Circuits

GENERAL COURSE INFORMATION

Dept.: ENGR	Course Num: 202	(Formerly:)
CIP Code: 14.1901	Intent Code:	Program Code:
Credits: 6		
Total Contact Hrs Per Qtr.: 88		
Lecture Hrs: 44	Lab Hrs: 44	Other Hrs: 0
Distribution Designation: Specified Elective SE		

COURSE DESCRIPTION (as it will appear in the catalog)
This course introduces students to the methods, skills and theoretical knowledge needed to design, simulate, and build combinational logic and basic sequential logic circuits. Using industry relevant CAD tools and design technologies, students will learn through homework and projects to design and implement a collection of combinational and sequential logic circuits. Upon completion, students will apply the same tools prevalent in industry and their transferrable skills to many digital electronic applications today.

PREREQUISITES
MATH& 141 with grades of 2.0 or higher, and one of the following: CS 111 or CS& 131 or CS&141, or instructor permission.

TEXTBOOK GUIDELINES
Open source textbook, lab project manual, lecture videos, power-points lecture notes, and free resources will be posted online (Canvas) for 24/7 access. Access to the internet will be required.

COURSE LEARNING OUTCOMES
Upon successful completion of the course, students should be able to demonstrate the following knowledge or skills:

1. Explain basic terminology related to electronic circuits and digital circuits.
2. Demonstrate understanding of binary state terminology, CMOS circuits and symbols, basic logic functions and logic circuits.
3. Analyze and design small scale combinational logic circuits.
4. Minimize and optimize combinational circuit designs.
5. Use relevant tools, technologies, and software for the analysis and design of logic circuits.
6. Incorporate medium scale integrated circuits, like decoders, multiplexers, shifters, and comparators, into circuit design.
7. Build arithmetic circuits including adders, subtractors, multipliers, and ALUs (arithmetic and logic units).
8. Analyze circuit delays and timing defects in combinational logic circuits.
9. Use basic memory circuits and devices including flip-flops, latches, registers, and counters.
10. Analyze and design simple sequential circuits.

INSTITUTIONAL OUTCOMES
None

COURSE CONTENT OUTLINE

I. Introduction to Basic Electronics – voltage, current, Ohm's Law; circuits (digital vs analog, physical vs model circuits); electronic components, Basic I/O: switches and leds; connectors; PCB and IC.
II. Introduction to Digital Circuits – truth table, logic gates and functions; transistors as switches; CMOS technology; introduction to Combinational Circuits; SOP and POS circuits; XOR and XNOR.
III. Introduction to Verilog HDL, FPGA architecture and CAD tools.
IV. Combinational Logic - Logic Minimization using Boolean Algebra, K-Map, K-Map with Don't Care and K-Map with Entered Variables.
V. Basic Combinational Logic Circuits: Multiplexors, Decoders, Encoders, 7 Segment Decoders, and Shifters.
VI. Performance of Combinational Logic Circuits: delay and glitches.
VII. Arithmetic Circuits: Binary Number System, Comparators, Adders, Subtractors, Multipliers, and introduction to ALU.
VIII. Sequential Logic Circuits: introduction to memory circuits, Latch, and Flip-Flop.
IX. Introduction to the design of Sequential Logic Circuits: State Diagram; structural implementation of State Diagram.
X. Introduction to Microprocessors

DEPARTMENTAL GUIDELINES *(optional)*
PO5 should be assessed: Students will be able to solve problems by gathering, interpreting, combining and/or applying information from multiple sources.

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DIVISION CHAIR APPROVAL **DATE**